REMARKS

Claims 1, 3-10, 12-20, 22, and 23 remain in this application. No claims have been added, cancelled, or amended. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §103(a) Rejection - Wasson

The Examiner has rejected claims 1, 3-10, 12-20, and 22-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,181,151 B1, issued to Wasson (hereinafter referred to as "Wasson"). The Applicants respectfully submit that the present claims are allowable over Wasson.

Claim 1 recites an apparatus comprising:
"***an integrated circuit, said integrated circuit including:***
a test controller *having an instruction register and a test access port finite state machine (TAP FSM), said test controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal;*
at least one logic unit controller;
a single test bus *directly coupled between the test controller and the at least one logic unit controller;*
at least one design-for-test-feature *coupled to the at least one logic unit controller; and*
a logic unit *coupled to the at least one design-for-test-feature*
wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said integrated circuit, said logic unit controller generates a local shift signal and a local load signal from the packet,
wherein said integrated circuit performs tests and generates test signals directly on said integrated circuit."

Firstly, Wasson does not teach or suggest an integrated circuit including the claimed test controller, at least one logic unit controller, single test bus, at least one design-for-test-feature, and logic unit. Wasson discusses an integrated circuit tester (see e.g., Title). FIG. 1 depicts in block diagram form an integrated circuit (IC) tester 10 in accordance with the invention (see e.g., column 3, lines 54-55). The IC tester 10 includes

a set of N tester channels CH(1)-CH(N) each carrying out test activities at a separate terminal of an IC device under test (DUT) 14 during a test (see e.g., column 3, lines 56-58). As understood by Applicants, the set of N tester channels CH(1)-CH(N) as well as other illustrated components of the IC tester shown in FIG. 1 are **external to the IC device under test (DUT) 14**. In any event, there is no teaching or reasonable suggestion of an integrated circuit that includes the claimed test controller, the at least one logic unit controller, the single test bus, the at least one design-for-test-feature, and the logic unit.

Secondly, there is no teaching or reasonable suggestion in Wasson of a test controller, which is included in an integrated circuit, that is to generate a first global control signal, where the global control signal is a packet that includes a shift signal and a load signal. In fact, Applicants have performed an electronic search of the text of Wasson and respectfully submit that **the word "packet" is not even mentioned in Wasson**. Further there is absolutely no teaching or reasonable suggestion whatsoever in Wasson of a test controller, which is included in an integrated circuit, that is to generate a first global control signal, where the global control signal is a packet that includes a shift signal and a load signal.

For at least these reasons, claim 1 is believed to be allowable over Wasson. Claims 3-9 depend from claim 1 and are believed to be allowable therefor, as well as for the recitations set forth in each of these dependent claims.

Independent claims 10 and 18, as well as their respective dependent claims, are also believed to be allowable.

35 U.S.C. §103(a) Rejection - Wasson

The Examiner has stated that the "design" limitation is also rejected under 35 USC 112, Second Paragraph, for being indefinite. Applicants respectfully submit that the

design limitation is not indefinite. As explained in the patent application on page 2 at lines 4-6, design for test features are known hardware features that may be incorporated into a chip to aid in testing and debugging.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8-22-05

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